In the Claims

1. (Previously Presented): A method of fabricating integrated circuitry comprising:

forming a conductive line having opposing sidewalls over a semiconductor substrate, the conductive line having an outer etch stop cap;

depositing an insulating layer over the substrate and the line;

planarize polishing the insulating layer using the outer etch stop cap as an etch stop;

after the planarize polishing, etching the insulating layer proximate the line along at least a portion of at least one sidewall of the line; and

after the etching, depositing an insulating spacer forming layer over the substrate and the line, and anisotropically etching it to form an insulating sidewall spacer along said portion of the at least one sidewall.

2. (Original): The method of claim 1 wherein the etching of the insulating layer is conducted along at least a portion of each of the opposing line sidewalls, the anisotropic etching forming an insulating sidewall spacer over each of the opposing line sidewalls.

3. (Original): The method of claim 1 wherein the etching of the insulating layer is conducted along the portion of the one sidewall and not along the opposing sidewall.

4. (Original): The method of claim 1 wherein the portion comprises a majority of said one sidewall.

5. (Original): The method of claim 1 wherein the portion comprises the substantial entirety of said at least one sidewall.

6. (Original): The method of claim 1 wherein the etching of the insulating layer outwardly exposes material of the semiconductor substrate.

7. (Original): The method of claim 1 wherein the conductive line is formed to comprise a transistor gate.

Claims 8-63 (Canceled).

64. (New): The method of claim 1 wherein the line comprises a transistor gate line.

65. (New): The method of claim 1 wherein the line does not comprise a transistor gate line.

66. (New): The method of claim 1 wherein the conductive line comprises conductively doped semiconductive material.

67. (New): The method of claim 1 comprising providing an insulative capping layer on the line, the outer etch stop cap being received over the insulative capping layer.

68. (New): The method of claim 67 wherein the etch stop cap comprises polysilicon.

69. (New): The method of claim 68 wherein the insulative capping layer comprises silicon dioxide.

70. (New): The method of claim 1 wherein the insulating layer comprises undoped silicon dioxide.

71. (New): The method of claim 1 wherein the insulating layer comprises doped silicon dioxide.

72. (New): The method of claim 71 wherein the insulating layer comprises borophosphosilicate glass.

73. (New): The method of claim 1 wherein the planarize polishing comprises chemical mechanical polishing.

74. (New): The method of claim 1 wherein the spacer forming layer comprises silicon nitride and the insulating layer comprises silicon dioxide.

75. (New): The method of claim 74 wherein the silicon dioxide is doped.

76. (New): The method of claim 74 wherein the silicon dioxide is undoped.

77. (New): The method of claim 1 comprising ion implanting into both of the insulative spacer and the insulating layer after the anisotropically etching.

78. (New): The method of claim 1 comprising forming a local interconnect layer over both of the insulative spacer and the insulating layer after the anisotropically etching.

79. (New): The method of claim 1 wherein the semiconductor substrate material comprises bulk substrate material.

80. (New): The method of claim 1 wherein the semiconductor substrate material comprises bulk monocrystalline silicon.

81. (New): The method of claim 1 comprising providing an insulative capping layer comprising silicon dioxide on the line, the outer etch stop cap being received over the insulative capping layer, and the outer etch stop cap comprising polysilicon on the silicon dioxide-comprising capping layer, and wherein the insulating layer comprises silicon dioxide.

82. (New): The method of claim 81 wherein the insulating layer comprises undoped silicon dioxide.

83. (New): The method of claim 81 wherein the insulating layer comprises doped silicon dioxide.

84. (New): The method of claim 83 wherein the insulating layer comprises borophosphosilicate glass.

85. (New): The method of claim 81 wherein the spacer forming layer comprises silicon nitride.

86. (New): The method of claim 82 wherein the spacer forming layer comprises silicon nitride.

87. (New): The method of claim 83 wherein the spacer forming layer comprises silicon nitride.

88. (New): The method of claim 84 wherein the spacer forming layer comprises silicon nitride.